REMARKS

Applicants thank the Examiner for the careful review of the present application and submit a Request for Continued Examination with these remarks. Further, Applicants amend independent claims 1, 9, 17 and 24 for clarification. The amended claims introduce no new matter and are fully supported by the specification.

The References and the Claimed Invention

Regarding the disclosed references in the final office action mailed on August 6, 2003, Vyoda et al. (U.S. Pub. 2002/0105057) and Yoon (U.S. Pub. 2002/0090784), Applicants respectfully submit that the combination of the two references do not teach the recited *methods*. Specifically, Applicants will describe the steps disclosed in Vyoda et al. in detail to illustrate the disclosed technology in contrast with the claimed invention.

What is Taught by Vyoda et al.

Under the summary of the invention, paragraph 8, Vyoda et al. discloses "[i]t is therefore an object of the present invention to provide a method and apparatus for forming a wafer surface comprising *semiconductor* that is hydrophilic *after a CMP process*." Continuing in paragraph 20, wafer 10 is shown as a cross section and top view in Figures 1A and 1B, respectively. Vyoda et al. teaches that "wafer 10...may be formed by *depositing* a semiconductor layer...on a substrate...and then *masking and selectively etching* the semiconductor layer to form elongated strips 11." Thereafter, "*a blanket layer* of dielectric...*may then be deposited on top* of strips 11." "Chemical mechanical planarization (CMP) may then be performed to remove excess dielectric to expose semiconductor regions

11 and to form dielectric regions 12." Further, in col. 2, paragraph 21, the reference discloses, "[a]fter the CMP removal step, residual particles including slurry particles and metal contaminants may remain on the surface of wafer 10. The residual slurry particles and metal contaminants may be removed during a wet cleaning step."

The reference also discloses on paragraph 36 that the wafer "may be formed by first depositing, selectively masking and etching a dielectric layer...and subsequently depositing a semiconductor layer on top of the dielectric regions. CMP may then be performed to remove excess semiconductor and to expose the surface of the dielectric regions."

Thus, Vyoda et al. teaches depositing a first layer, masking and etching the first layer, depositing a second layer, applying CMP to the second layer and then wet cleaning the layers. Based on these steps, it is important to note that the *etched first layer has been filled* by the second layer, *followed by a CMP process* of the second layer prior to wet cleaning.

The Claimed Invention

In contrast, the recited methods include "plasma etching a feature into a low K dielectric layer...ashing the semiconductor wafer...the ashing generating ashing residues...and removing the etching residues and ashing residues from the low K dielectric layer." Each independent claim recites a similar process of etching, ashing, and removing etching and ashing residues. These methods are distinctly different from Vyoda et al. because the methods recited in the claims would not produce a wafer surface requiring CMP before the "removing" operation. Specifically, *after etching and ashing, the etched features are not yet filled.* Thus, during the claimed invention's scrubbing operation, the cleaning chemistry and wetting agent *enter the non-filled etched features* while in the Vyoda et al. cleaning step, the

cleaning chemistry can never enter the etched features because the etched features have already been filled and planarized.

The amended independent claims now recite, "the low K dielectric having the plasma etched feature." The clarifying amendments distinctly point out how the *plasma etched feature* is subjected to the *removing* operation by scrubbing the low K dielectric layer with a wet brush. In Vyoda et al., the etched features are filled and planarized before wet cleaning, and thus it is not possible to clean the etched features prior to filling. Accordingly, the amended claims recite an element not taught or suggested by Vyoda et al.

Moreover, from the standpoint of the overall wafer fabrication process, the steps disclosed in Vyoda et al. do not describe the operations recited by Applicants' independent claims. Vyoda et al. skips and makes no mention of ashing etched features, nor describes how to remove residues from the etched and ashed features prior to deposition of a second layer. Particularly, the steps disclosed in Vyoda et al. teach how to clean a CMP planarized surface with a filled etch feature. Because Vyoda et al. teaches steps later in the wafer fabrication process and further, fails to mention the operations recited in Applicants' independent claims, Vyoda et al. does not teach or suggest how to clean post-etch and strip residues from a wafer as recited by Applicants' claims.

Accordingly, because Vyoda et al. singly or in combination with Yoon cannot teach or suggest a method for the invention, Applicants respectfully submit that independent method claims 1, 9, 17 and 24 are allowable. Because the independent claims are submitted to be allowable, the dependent claims, which depend from the independent claims, are submitted to be allowable for the same reason. Accordingly, Applicants respectfully request a notice of allowance for pending claims 1-24.

If the Examiner has any questions, please contact the undersigned at (408) 749-6900, ext. 6911. Further, if any fees are due in connection with filing this amendment, the Commissioner is authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P316). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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